**In the Claims**

Please replace the claims with the following clean version of the entire set of pending claims. Cancel all previous versions of any pending claim. A marked-up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment. Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

## CLAIMS

21. DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate the first and second capacitor electrodes, the region comprising aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines.

22. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of aluminum nitride.

23. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

24. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 60 Angstroms.

25. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

26. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

27. (Amended) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 60 Angstroms.

28. The circuitry of claim 21 wherein the aluminum nitride is substantially amorphous.

**New Claims:**

Add new claims 64-75 as follows:

64. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of substantially amorphous aluminum nitride.

65. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

66. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 60 Angstroms.

67. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

68. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

69. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 60 Angstroms.

70. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

71. (Added) The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

72. (Added) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

73. (Added) The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

74. (Added) The circuitry of claim 21 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

75. (Added) The circuitry of claim 28 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.